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web as an alternative you can also write your simulation stimulus using generic vhdl code called a testbench the testbench codes gets compiled along with the design so that the stimulus is also in the compiled simulation model ieee came along and created additional libraries that are supported by almost all vhdl compilers specific silicon

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pair or one entity with multiple architectures the entity section of the hdl design is used to declare the i o ports of the circuit while the description code resides within architecture portion

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